

## ABSTRACT

A dynamic random access memory (DRAM) cell and associated array are disclosed. The DRAM cell (300) includes a storage capacitor (304) and a pass transistor (302). The pass transistor (302) includes a source region (322), drain region (320) and channel region (324). A top gate (318) is disposed over the channel region (324) and a bottom gate (310) is disposed below the channel region (324). The top gate (318) and bottom gate (310) are commonly driven to provide greater control of the pass transistor (302) operation, including an off state with reduced source-to-drain leakage. The DRAM array (400) includes memory cells (414) having pass transistors (500) with double-gate structures. Memory cells (414) within the same row are commonly coupled to a top word line and bottom word line. The resistance of the top and bottom word lines is reduced by a word line strap layer (600). The DRAM array (400) further includes a strapping area that is void of memory cells. Conductive contact between the top word line, bottom word line, and word line strap layer (600) of each row is made within the strapping area by way of strapping vias (604) and top-to-bottom word line vias (602).